Hotswap, Inrush Current Limiter Controllers (Negative Supply Rail)

Not Recommended for New Designs

Features

- PWRGD = Active Low
- -10V to -90V input voltage range
- Few external components
- 0.33mA typical standby supply current
- Programmable over/under voltage limits with hysteresis
- Programmable current limit
- Active control during all phases of start-up
- Programmable timing
- 8-Lead SOIC package

Applications

- Central office switching
- Servers
- POTS line cards
- ISDN line cards
- xDSL line cards
- PBX Systems
- Powered Ethernet for VoIP
- Distributed power systems
- Negative power supply control
- Antenna and fixed wireless systems

General Description

The Supertex HV310, Hotswap Controller, Negative Supply controls the power supply connection during insertion of cards or modules into live backplanes. It may be used in traditional 'negative 48V' powered systems or for higher voltage busses up to negative 90V.

Operation during the initial power up prevents turn-on glitches, and after complete charging of load capacitors (typically found in filters at the input of DC-DC converters) the HV310 issues a power good signal. This signal is typically used to enable the DC-DC converter. Once a $\overline{\text{PWRGD}}$ signal has been established, the device sleeps in a low power state, important for large systems with many individual hotswap cards or modules.

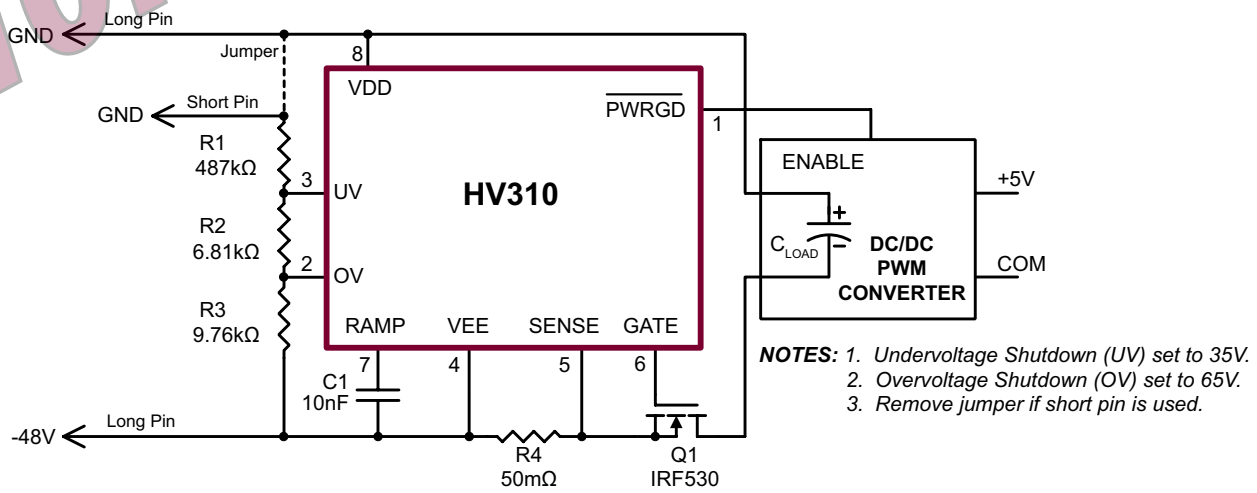
An external power MOSFET is required as the pass element, plus a ramp capacitor, and resistors to establish current limiting and over and under voltage lockouts. There is no need for additional external snubber components.

Features are programmable over voltage and under voltage detection of the input voltage which locks out the load connection if the bus (input) voltage is out of range. An internal voltage regulator creates a stable reference, and maintains accurate gate drive voltage. The unique control loop scheme provides full current control and limiting during start up.

Theory of Operation

Initially the external N-channel MOSFET is held off by the gate signal, preventing an input glitch. After a delay (while internal circuits are activated) the inrush current to the load is limited by the gate control output. The current may ramp up and limit at a maximum value programmed by an external resistor. Initial time delay, to allow for contact bounce, and charging operation is determined by the single external ramp capacitor connected to the RAMP pin. When the load capacitor is fully charged, the controller emerges from current limit mode, an additional time delay occurs before the external N-channel MOSFET pass transistor is switched to full conduction, and the $\overline{\text{PWRGD}}$ output signal is activated. The controller will then transition to a low power standby mode.

Typical Application Circuit



NOTES: *1. Undervoltage Shutdown (UV) set to 35V.*
2. Overvoltage Shutdown (OV) set to 65V.
3. Remove jumper if short pin is used.

Ordering Information

Device	Package Option
	8-Lead SOIC *4.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV310	HV310LG-G

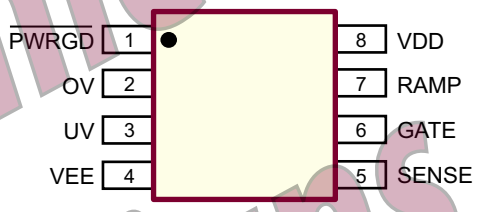
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{EE} referenced to VDD pin	+0.3 to -100V
V_{PWRGD} referenced to V_{EE} voltage	-0.3 to +100V
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
UV and OV referenced to V_{EE}	-0.3 to +12V

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



8-Lead SOIC (LG)
(top view)

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Electrical Characteristics *(V_{IN} = -10 to -90V, -40°C ≤ T_A ≤ +85°C unless otherwise noted)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Supply *(Referenced to VDD pin)*						
V_{EE}	Supply voltage	-90	-	-10	V	---
I_{EE}	Supply current	-	550	650	µA	V_{EE} = -48V, mode = limiting
	Standby mode supply current	-	330	400	µA	V_{EE} = -48V, mode = standby
OV and UV Control *(Referenced to VEE pin)*						
V_{UVH}	UV high threshold	-	1.26	-	V	Low to high transition
V_{UVL}	UV low threshold	-	1.16	-	V	High to low transition
V_{UVHY}	UV hysteresis	-	100	-	mV	---
V_{OVH}	OV high threshold	-	1.26	-	V	Low to high transition
V_{OVL}	OV low threshold	-	1.16	-	V	High to low transition
V_{OVHY}	OV hysteresis	-	100	-	mV	---

Not Recommended for New Designs

Electrical Characteristics *(V_{IN} = -10 to -90V, -40°C ≤ T_A ≤ +85°C unless otherwise noted)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Current Limit *(Referenced to VEE pin)*						
V_{SENSE}	Current limit threshold voltage	40	50	60	mV	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
Gate Drive Output *(Referenced to VEE pin)*						
V_{GATE}	Maximum GATE drive voltage	9.0	10	11	V	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
I_{GATEUP}	GATE drive pull-up current	500	-	-	µA	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
$I_{GATEDOWN}$	GATE drive pull-down current	40	-	-	mA	$V_{UV} = V_{EE}$, $V_{OV} = V_{EE} + 0.5V$
Timing Control *(Test Conditions: C =100µF, C_{RAMP} = 10nF, $V_{UV} = V_{EE}$ +1.9V, $V_{OV} = V_{EE}$ +0.5V, External MOSFET is IRF530[3])*						
I_{RAMP}	Ramp pin output current	-	10	-	µA	V_{SENSE} = 0V
t_{POR}	Time from UV to GATE turn on[1]	2.0	-	-	ms	---
t_{RISE}	Time from GATE turn on to V_{SENSE} limit	400	-	-	µs	---
t_{LIMIT}	Duration of current limit mode	-	-	5.0	ms	---
t_{PWRGD}	Time from current limit to PWRGD	-	5.0	-	ms	---
V_{RAMP}	Voltage on ramp pin in current limit mode[2]	-	3.6	-	V	---
Power Good Output *(Referenced to VEE pin)*						
V_{PWRGD}	Power good pin breakdown voltage	90	-	-	V	---
	Power good pin output low voltage	-	0.5	0.8	V	I_{PWRGD} = 1.0mA
Dynamic Characteristics						
$t_{GATEHLOV}$	OV delay	-	-	500	ns	---
$t_{GATEHLUV}$	UV delay	-	-	500	ns	---

Notes

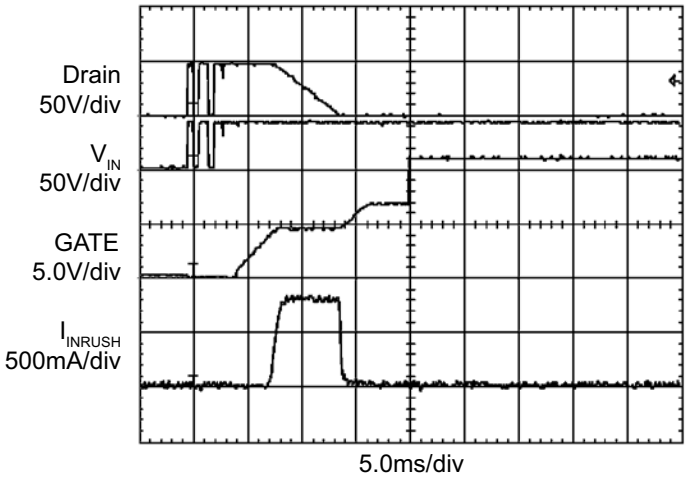
1. *This timing depends on the threshold voltage of the external N-Channel MOSFET. The higher its threshold is, the longer this timing.*
2. *This voltage depends on the characteristics of the external N-Channel MOSFET. $V_{GS(th)}$ = 3.0V for an IRF530.*
3. *IRF530 is a registered trademark of International Rectifier.*

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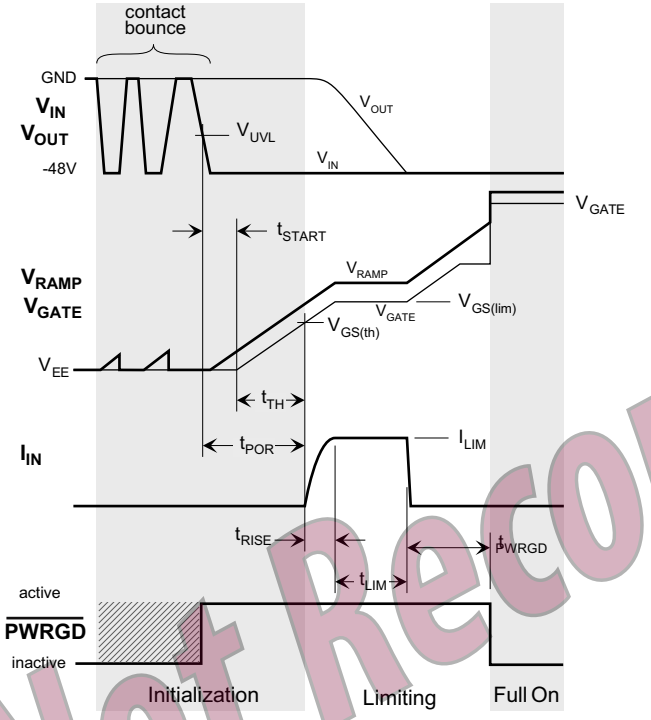
PWRGD Logic

Device	Condition	PWRGD	
HV310	Not Ready	1	Hi Z
	Ready	0	V_{EE}

Waveforms



Timing Diagram



$$I_{LIM} = \frac{V_{SENSE}}{R_{SENSE}}$$

$$t_{START} = 12V \frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{TH} = V_{GS(th)} \frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{POR} = t_{START} + t_{TH}$$

$$t_{RISE} \approx \frac{C_{RAMP}}{g_{fs}\left[\frac{I_{RAMP}}{0.9I_{LIM}} - \frac{R_{SENSE}}{R_{FB}}\right]}$$

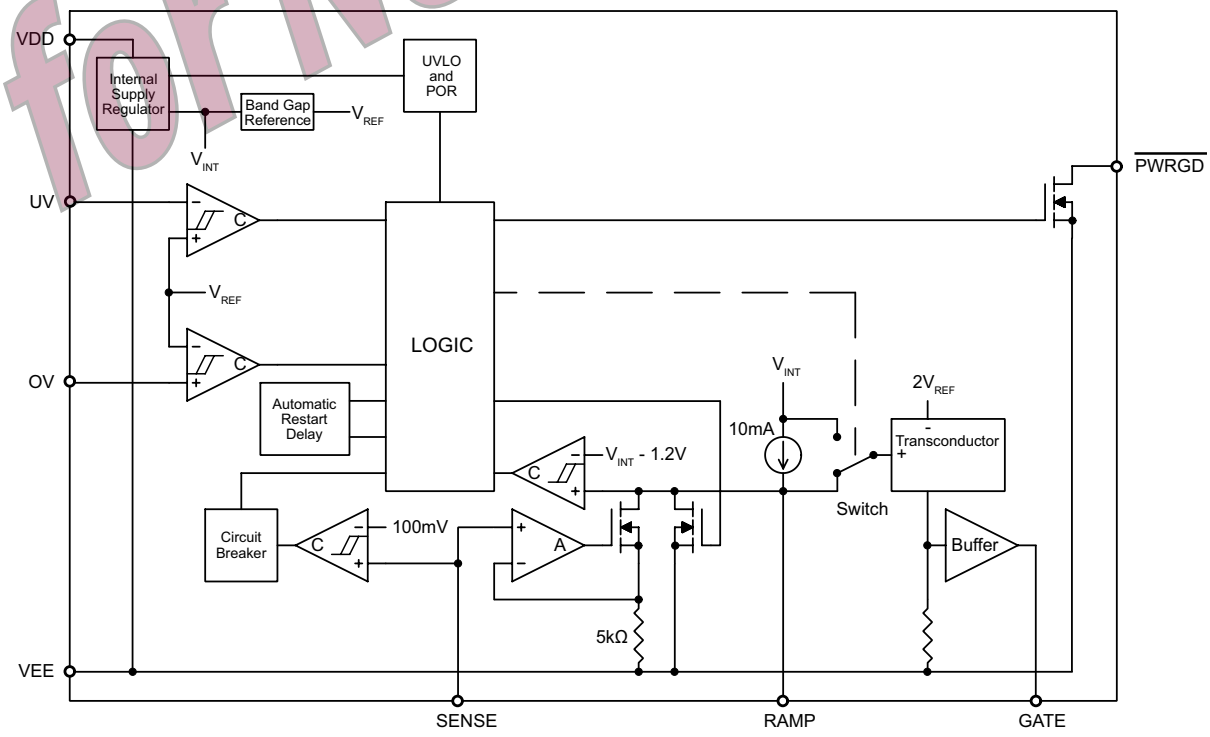
$$t_{LIM} \approx V_{IN} \frac{C_{LOAD}}{I_{LIM}} - \frac{1}{2} t_{RISE}$$

$$t_{PWRGD} = (V_{INT} - V_{GS(LIM)} - 1.2V) \frac{C_{RAMP}}{I_{RAMP}}$$

Note:

1. *V_{INT} is the internally regulated supply voltage and can range from 9.0 to 11V.*
2. *$V_{GS(th)}$ is the gate threshold voltage of the external pass transistor and may be obtained from its datasheet.*
3. *$V_{GS(lim)}$ is the pass transistor gate-source voltage required to obtain the limit curent. It is dependent on the pass transistor's characteristics and may be obtained from the transfer characteristics curves on the transistor datasheet.*
4. *g_{fs} is the transconductance of the pass transistor and may be obtained from its datasheet.*
5. *R_{FB} is the internal feedback resistor and is 5.0kΩ nominal.*

Functional Block Diagram



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Functional Description

Insertion Into Hot Backplanes

Telecom, Data Network and some computer applications require the ability to insert and remove circuit cards from systems without powering down the entire system. All circuit cards have some filter capacitance on the power rails, which is especially true in circuit cards or network terminal equipment utilizing distributed power systems. The insertion can result in high inrush currents that can cause damage to connector and circuit cards and may result in unacceptable disturbances on the system backplane power rails.

The HV310 was designed to allow the insertion of these circuit cards or connection of terminal equipment by eliminating these inrush currents and powering up these circuits in a controlled manner after full connector insertion has been achieved. The HV310 is intended to provide this function on a negative supply rail in the range of -10 to -90V.

Operation

On initial power application an internal regulator seeks to provide 10V for the internal IC circuitry. Until the proper internal voltage is achieved all circuits are held reset, the open drain PWRGD signal is Hi-Z to inhibit the start of any load circuitry and the gate to source voltage of the external N-channel MOSFET is held low. Once the internal under voltage lock out (UVLO) has been satisfied, the circuit checks the input supply voltage under voltage (UV) and over voltage (OV) sense circuits to ensure that the input voltage is within acceptable programmed limits. These limits are determined by the selected values of resistors R1, R2 and R3, which form a voltage divider.

Assuming the above conditions are satisfied and while continuing to hold the PWRGD output inactive and the external MOSFET GATE voltage low, the current source feeding the RAMP pin is turned on. The external capacitor connected to it begins to charge, thus starting an initial time delay determined by the value of the capacitor. If an interruption of the input power occurs during this time (i.e. caused by contact bounce) or the OV or UV limits are exceeded, an immediate reset occurs and the external capacitor connected to the RAMP pin is discharged.

When the voltage on the RAMP pin reaches an internally set voltage limit, the gate drive circuitry begins to turn on the external MOSFET; allowing the current to softly rise over a period of a few hundred micro-seconds to the current limit set point. While the circuit is limiting current, the voltage on the RAMP pin will be fixed.

Depending on the value of the load capacitance and the programmed current limit, charging may continue for some time. The magnitude of the current limit is programmed by comparing a voltage developed by a sense resistor connected between the VEE and SENSE pins to 50mV (Typical). Once the load capacitor has been charged, the current will drop which will cause the ramp voltage to continue rising; providing yet another programmed delay.

When the ramp voltage is within 1.2V of the internally regulated voltage, the controller will force the GATE full on and will pull the $\overline{\text{PWRGD}}$ pin low and the circuit will transition to a low power standby mode. The $\overline{\text{PWRGD}}$ pin is often used as an enable for downstream DC/DC converter loads.

At any time during the start up cycle or thereafter, crossing the UV and OV limits (including hysteresis) will cause an immediate reset of all internal circuitry. Thereafter the start up process will begin again.

Application Information

Under Voltage and Over Voltage Detection

The UV and OV pins are connected to comparators with nominal 1.21V thresholds and 100mV of hysteresis (1.21V ± 50mV). They are used to detect under voltage and over voltage conditions at the input to the circuit. Whenever the OV pin rises above its threshold or the UV pin falls below its threshold the GATE voltage is immediately pulled low, the PWRGD signal is deactivated and the external capacitor connected to the RAMP pin is discharged.

The under voltage and over voltage trip points can be programmed by means of the three resistor divider formed by R1, R2 and R3. Since the input currents on the UV and OV pins are negligible the resistor values may be calculated as follows:

$$UV_{OFF} = V_{UVH} = 1.16 = |V_{EEUV}| \bullet (R2+R3) / (R1+R2+R3)$$
$$OV_{OFF} = V_{OVL} = 1.26 = |V_{EEOV}| \bullet R3 / (R1+R2+R3)$$

Where $|V_{EEUV}|$ and $|V_{EEOV}|$ are Under & Over Voltage Set points.

If we select a divider current of 100µA at a nominal operating input voltage of 50V then:

$$(R1+R2+R3) = 50V / 100\mu A = 500k\Omega$$

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From the second equation for an over voltage set point of 65V, the value of R3 may be calculated.

OV_{OFF} = 1.26 = 65 • R3 / 500kΩ
R3 = (1.26 • 500K) / 65 = 9.69 kΩ

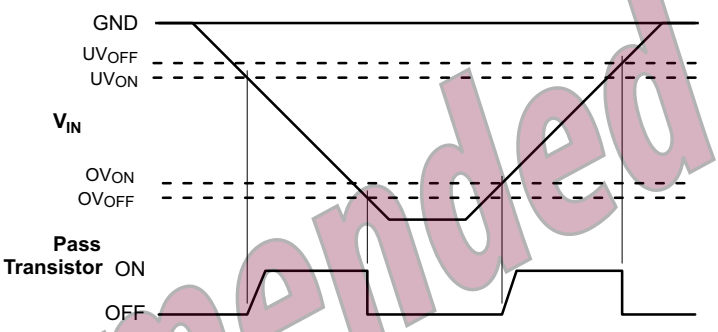
The closest 1% value is 9.76kΩ.

From the first equation for an under voltage set point of 35V, the value R2 can be calculated.

UV_{OFF} = 1.16 = 35 • (R2 + R3) / 500K
R2 = (1.16 • 500K) / 35 – 9.76kΩ = 6.81kΩ.
The closest 1% value is 6.81kΩ.

Then R1 = 500K – (R2 + R3) = 483kΩ
The closest 1% value is 487kΩ.

Undervoltage/Overvoltage Operation



Current Limit

The current limit magnitude above which the current will not be allowed to rise during startup is programmed using a sense resistor connected from the SENSE pin to VEE pin. For example to program a current limit of 1.0A, one would choose a resistor as follows:

R_{SENSE} = 50mV / I_{SENSE}
R_{SENSE} = 50mV / 1.0A
R_{SENSE} = 50mΩ

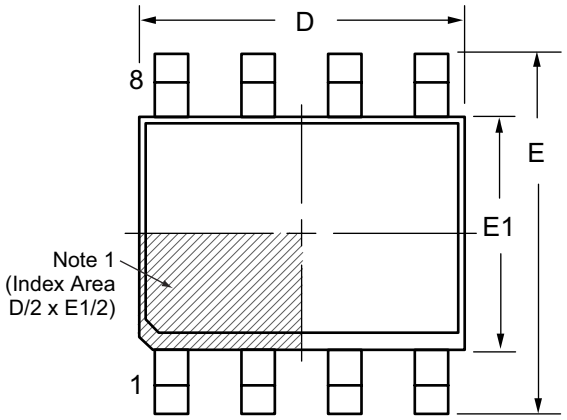
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Pin Description

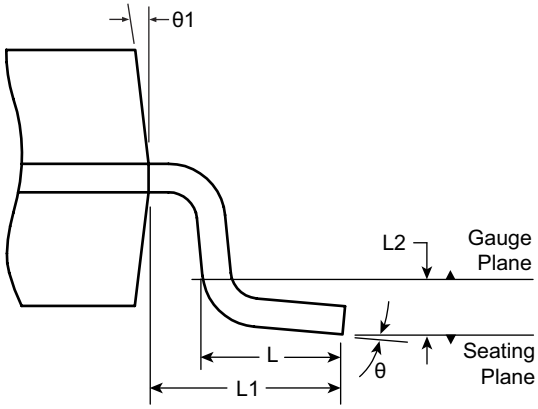
Pin #	Function	Description
1	$\overline{\text{PWRGD}}$	Ths pin is held in Hi-Z state on initial power application and pulls low when the external MOSFET is fully turned on. This pin may be used as an enable control when connected directly to a PWM power module.
2	OV	This pin, when raised above its high threshold, will immediately cause the GATE pin to be pulled low. The GATE pin will remain low until the voltage on this pin falls below the low threshold limit, initiating a new start-up cycle.
3	UV	This Under Voltage sense pin, when below its low threshold limit will ensure that the GATE pin is low. The GATE pin will remain low until the voltage on this pin rises above the high threshold, initializing a new start-up cycle.
4	VEE	This pin is the negative voltage power supply input to the circuit.
5	VDD	This pin is the positive voltage power supply input to the circuit.
6	RAMP	This pin provides a current output so that a timing ramp voltage is generated when a capacitor is connected. The initial portion of the ramp provides a time delay, which in conjunction with the Under Voltage detection circuit eliminates circuit card insertion contact bounce. The RAMP pin also controls the delay between the current limit mode disengaging and the PWRGD signal activating; as well as the current rise profile after the initial turn on delay.
7	GATE	This is the GATE driver output for the external N-Channel MOSFET.
8	SENSE	The current sense resistor connected from this pin to VEE pin programs the current limit. Constant current output mode is established when the voltage drop across this resistor reaches 50mV.

8-Lead SOIC (Narrow Body) Package Outline (LG)

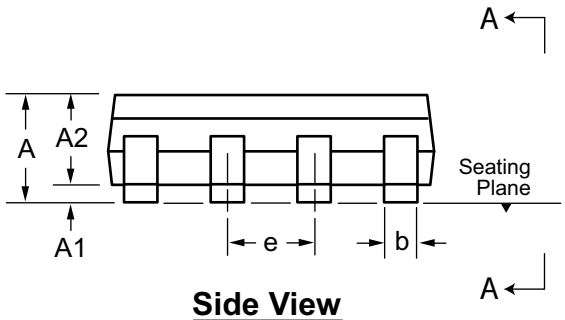
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



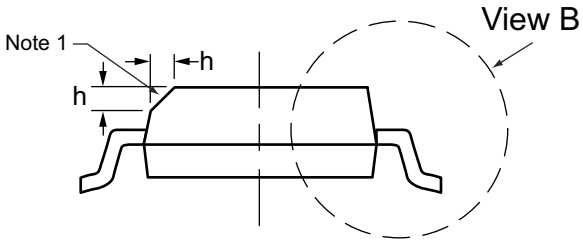
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-8SOLGTG, Version H101708.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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